L Number	Hits	Search Text	DB	Time stamp
1	4487	implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))	USPAT; US-PGPUB	2002/07/03 15:47
2	3905	(implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))) and (via or trench or hole or opening or groove)	USPAT; US-PGPUB	2002/07/03 15:51
3	144	((implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))) and (via or trench or hole or opening or groove)) and damascene	USPAT; US-PGPUB	2002/07/03 15:52
4	112	(((implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))) and (via or trench or hole or opening or groove)) and damascene) and @ad<=20001206	USPAT; US-PGPUB	2002/07/03 15:21
5	1913	implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))	EPO; JPO; DERWENT; IBM_TDB	2002/07/03 15:47
6	795	(implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))) and (via or trench or hole or opening or groove)	EPO; JPO; DERWENT; IBM_TDB	2002/07/03 15:52
7	9	((implant$5 with (dielectric or insulating) and ((etching or removing) with (dielectric or insulating))) and (via or trench or hole or opening or groove)) and damascene	EPO; JPO; DERWENT; IBM_TDB	2002/07/03 15:52

DOCUMENT-IDENTIFIER: US 6372660 B1
TITLE: Method for patterning a dual damascene with masked implantation

---------- KWIC ---------

ABPL:
A substrate is provided, and a first dielectric layer is formed, thereon. Then a first photoresist layer is formed and defined on the first dielectric layer. Next, a dense region as an etched barrier layer is formed in the first **dielectric** layer by an ion **implantation** with photoresist layer as a mask. A second dielectric layer is formed on the first dielectric layer after the first photoresist layer is removed. Afterward forming a second photoresist layer on the second dielectric layer and defining a predetermined trench region to expose a partial surface of the second dielectric layer, wherein the partial surface of the second dielectric layer comprises the dense region. Subsequently, an etching process is performed by means of the second photoresist layer as an etched mask to etch through the second **dielectric** layer and the first **dielectric** layer until the substrate surface is exposed for patterning the dual damascene.

BSPR:
There are two methods for conventional via and interconnect processes, one method is that via and interconnect finish by oneself, wherein the method is that the **dielectric** is first formed on the metal layer, and then the photoresist layer (PR) is defined on the **dielectric, and use the etching** process to make the via, and deposit conduction material in the via by means of

deposition to finish the via process, then deposit and define metal layer,
afterward deposit the **dielectric** layer whereon. Conventional process forming
the metal interconnect is that make the via window and the interconnect by
means of two lithography process. Thus, it is need cumbrous steps of deposit
and pattern. And yet, it will result in interconnects to be difficult
patterned due to the multi layer connect layout is more daedal in the
sub-quarter micron.

BSPR:
Conventional dual damascene include two patterns, one is the deep patterns,
that is the via patterns; another is the shallow patterns or the line patterns,
that is the trench patterns. Conventional via first process for forming a dual
damascene is shown as FIG. 1A to FIG. 1C, first of all, a first **dielectric**
layer 110, an etching stop layer 120 and a second **dielectric** layer 130 are
formed on the substrate 100 in order. Then a first photoresist layer 140 is
formed on the second dielectric layer 130, and the first photoresist layer 140
is defined and patterned as a deep pattern area. Next, performing an etching
process of the deep patterns by means of the first photoresist layer 140 as a
etched mask, and then punching through the second **dielectric** layer 130, etching
stop layer 120 and the first **dielectric** layer 110, while a via hole 150 is
formed. After removing the first photoresist layer 140, a second photoresist
layer 160 is formed on the second **dielectric** layer 130, and it is defined to
form a shallow pattern area and expose the partial surface of the via hole 150
and the second **dielectric** layer 130 so that the horizontal size of the shallow
patterns is large more then one of the deep patterns. Afterward performing an

etching process of the shallow patterns by means of the second photoresist
layer 160 as an etched mask and the etching stop layer 120 as an etching
terminal point, so as to remove exposed partial surface of the second
dielectric layer 130 and form a trench 170 having large horizontal size.
Subsequently, the second photoresist layer 160 is removed to form the opening
of the damascene 150 and 170. Final, proceed a interconnect process, since the
above processes are well known in the prior art, which are not the focus of the
present invention, hence will not be described in greater details.

BSPR:
Likewise, conventional trench first process for forming a dual damascene is
shown as FIG. 2A to FIG. 2C, first of all, a first **dielectric** layer 210, an
etching stop layer 220 and a second **dielectric** layer 230 are formed on the
substrate 200 in order. Then a first photoresist layer 240 is formed on the
second dielectric layer 230, and then it is defined to form a shallow pattern
area and expose the partial surface of the second dielectric layer 230. Next,
performing an etching process of the shallow patterns by means of the first
photoresist layer 240 as an etched mask and the etching stop layer 220 as an
etching terminal point, so as to remove exposed partial surface of the second
dielectric layer 230 and form a trench 270. After removing the first
photoresist layer 240, a second photoresist layer 260 is formed on the second
dielectric layer 230 and the first **dielectric** layer 210, and then it is defined
to form a shallow pattern area and expose the partial surface of the first
dielectric layer 210 so that the horizontal size of the shallow patterns is
large more then one of the deep patterns. Afterward

performing an etching
process of the deep patterns by means of the second photoresist layer 260 as an
etched mask to form a trench 270 having a smaller horizontal size.
Subsequently, the second photoresist layer 260 is removed to form the opening
of the damascene 250 and 270. Final, proceed a interconnect process, since the
above processes are well known in the prior art, which are not the focus of the
present invention, hence will not be described in greater details.

BSPR:
Likewise, conventional embedded hard mask process for forming a dual damascene
is shown as FIG. 3A to FIG. 3D, first of all, a first dielectric 310 and an
embedded hard mask layer 320 are formed on the substrate 300 in order. Then a
first photoresist layer 330 is formed on the embedded hard mask layer 320, and
then it is defined to form a first predetermined etched area and expose the
partial surface of the embedded hard mask layer 320. Next, performing an
etching process by the first photoresist layer 330 as an etched mask to etch
the first predetermined etched region and remove exposed partial surface of the
embedded hard mask layer 320, and then form an etched region 340 on the first
dielectric layer 310. After removing the first photoresist layer 330, a second
dielectric layer 350 is formed on the first **dielectric** layer 310, and it is
filled into the etched region 340. Subsequently, a second photoresist layer
360 is formed on the second dielectric layer 350 and it is defined to form a
second predetermined etched region, which has the etched region 340, so that a
partial surface of the second dielectric layer 350 is exposed. Afterward
performing an etching process of the deep patterns by means of the second

photoresist layer 360 as an etched mask to etch the second predetermined etched region, and then etching through the second **dielectric** layer 350 and the first **dielectric** layer 310, so as to form a trench 370 and a via hole 380. The second photoresist layer 360 is then removed to form the opening of the damascene 370 and 380. Final, proceed a interconnect process, since the above processes are well known in the prior art, which are not the focus of the present invention, hence will not be described in greater details.

BSPR:
The skill of the dual damascene is a method for forming via and interconnects.
In the conventional dual damascene skill of above, it is necessary that the etching stop layer or the embedded hard mask have to be formed between two **dielectric** layers to perform the etching process. Therefore, there is a large fabricated cost due to the complex step for forming a dual damascene with conventional process. Moreover, performance of device is affected because the addition of etching stop layer or the embedded hard mask makes **dielectric** constant (K) to raise. Further, there are interface or adherence issues during forming multi-layer with various materials.

BSPR:
Furthermore, in the via first process, it is necessary that the **dielectric** layer has enough thickness, so as to avoid damaging semiconductor substrate during over-etching process for forming the via hole, but if the thickness of the **dielectric** layer is raised, the **dielectric** constant will be increased, and that device dimension, in sub-micron process, is difficult to be decreased.
Hence, a protected layer, such as organic polymer, has to be added on the

dielectric before forming the trench. Nevertheless, the organic material is difficult to remove so that process is very hard. Likewise, in the trench first process, there are depth of focus (DOF) issue or critical dimension (CD) issue that is difficult to control. On the other hand, both the etching process of the via first process and the trench first process is performed on the different surface, so that the process window is difficult to control after etching.

BSPR:
Still another object of the present invention is that provide a new method for patterning the dual damascene. In this invention, a dense region as an etched barrier layer is formed in the **dielectric** layer by an ion **implantation**, so as to substitute for the embedded hard mask or the etched stop layer in the conventional process. Hence, the method of this invention is suitable for use in the sub micron.

BSPR:
In accordance with the present invention, a new method for forming the dual damascene is disclosed. In one embodiment of the present invention, first of all, a substrate is provided, and a first dielectric layer is formed, thereon. Then a first photoresist layer is formed and defined on the first dielectric layer. Next, a dense region as an etched barrier layer is formed in the first **dielectric** layer by an ion **implantation** with photoresist layer as a mask. A second dielectric layer is formed on the first dielectric layer after the first photoresist layer is removed. Afterward forming a second photoresist layer on the second dielectric layer and defining a predetermined trench region to expose a partial surface of the second dielectric layer,

wherein the partial
surface of the second dielectric layer comprises the dense region.
Subsequently, an etching process is performed by means of the second
photoresist layer as an etched mask to etch through the second **dielectric** layer
and the first **dielectric** layer until the substrate surface is exposed for
patterning the dual damascene. Finally, removing the second photoresist layer
and performing a interconnect process, since the above processes are well known
in the prior art, which are not the focus of the present invention, hence will
not be described in greater details.

DEPR:
As illustrated in FIG. 4A and FIG. 4B, in the first embodiment of the present
invention, first of all, a substrate 400 is provided and a dielectric layer 410
is formed over the substrate 400. Then a photoresist layer 420 is formed and
defined on the dielectric layer 410. Next, a uniform dense region 440 is
formed in the **dielectric** layer 410 by an ion **implantation** process 430 with the
photoresist layer 420 as a mask. The ion implantation process 430 of above,
which is a physical method, can bombard material with ions to change the
material density, such as the uniform dense region 440, and it is as etched
barrier layer in follow-up etching process. The ion implantation process 430
is a masked implantation that uses phosphorous (P), arsenic (As) or BF.sub.2
ions, whose dosage is about between 10.sup.12 and 10.sup.15, with energy about
between 20 KeV and 100 KeV. However, it should be noted that the ion
implantation process 430 is not limited to implement the number of times and
the conditions in above specific embodiment.

DEPR:

Referring to FIG. 5A, in the second embodiment of the present invention, first of all, a substrate 500 is provided, and a first dielectric layer 510 is deposited, thereon, wherein the batter material of the first dielectric layer 510 is a low-K dielectric material and the batter thickness of the first dielectric layer 510 is about 4000 to 6000 .ANG.. Then a first photoresist layer 520 is formed and defined on the first dielectric layer 510. Next, a uniform dense region 540 as a etched barrier layer is formed in the first **dielectric** layer 510 by a masked **implantation** 530 and the first photoresist layer 520 as an ion **implanted** mask, wherein the thickness of the uniform dense region 540 is about 1000 .ANG. to 2000 .ANG.. The masked implantation 530 of above is performed by an ion, such as phosphorous (P), arsenic (As) or BF.sub.2 ion, having dosage about 10.sup.12 to 10.sup.15.

DEPR:
Referring to FIG. 5B, in this embodiment, a second dielectric layer 550 is deposited on the first dielectric layer 510 after the first photoresist layer 520 is removed, wherein the batter material of the second dielectric layer 550 is a low-K dielectric material and the batter thickness of the second dielectric layer 550 is about 4000 to 6000 .ANG.. Afterward forming a hard mask layer 560 on the second dielectric layer 550, and then forming and defining a second photoresist layer 570 on the hard mask layer 560 to expose a partial surface of the hard mask layer 560 as a predetermined etched region, wherein the location of partial surface on the hard mask layer 560 comprises the location of uniform dense region 540. Subsequently, an etching process is performed by means of the second photoresist layer 570 as an etched mask to

etch through the hard mask layer 560, the second **dielectric** layer 550 and the first **dielectric** layer 510 until surface of the substrate 500 is exposed for patterning the dual damascene. Final, removing the second photoresist layer 570 to form a trench 580 and a via hole 590 of the dual damascene, as shown in FIG. 5C.

DEPR:
Referring to FIG. 6A, in the third embodiment of the present invention, first of all, a substrate 600 is provided, and a first dielectric layer 610 is deposited, thereon. Then a first photoresist layer 620 is formed and defined on the first dielectric layer 610. Next, an etched barrier layer 640 is formed in the first **dielectric** layer 610 by an ion **implantation** 630 and the first photoresist layer 620 as a mask.

DEPR:
Referring to FIG. 6B, in this embodiment, a second dielectric layer 650 is formed on the first dielectric layer 610 after the first photoresist layer 620 is removed. Afterward forming and defining a second photoresist layer 660 on the second dielectric layer 650 to expose a partial surface of the second dielectric layer 650 as a predetermined etched region, wherein the location of partial surface on the second dielectric layer 650 comprises the location of the etched barrier layer 640. Subsequently, an etching process is performed by means of the second photoresist layer 660 as an etched mask to etch through the second photoresist layer 660 and the first **dielectric** layer 610 until surface of the substrate 600 is exposed for patterning the dual damascene. Finally, removing the second photoresist layer 660 to form a trench 670 and a via hole 680 of the dual damascene, as shown in FIG. 6C.

DEPR:
In these embodiments of the present invention, a new pattern method of the dual damascene is provided. The present invention uses the etching process with one time on the same surface, so as to control the process window and avoid the issues, such as DOF or CD. Hence, it is effective in raising quality of the process. Furthermore, it is unnecessary for forming the etched stop layer or the embedded hard mask, so as to avoid increasing dielectric constant due to increase the thickness of dielectric layer or the addition of the etched stop layer. Accordingly, this invention can raise performance of logic circuit.
Moreover, the present invention can also prevent issues of interface or adherence. Therefore, it is possible to provide a highly reliable semiconductor device without the occurrence of deterioration of interconnects quality. Further, it can simplify step of process to reduce fabrication cost.
In other words, the method of the present invention is easily and to conform to the economic effect. On the other hand, in this invention, a dense region as an etched barrier layer is formed in the **dielectric** layer by the masked **implantation**, so as to substitute for the embedded hard mask or the etched stop layer in the conventional process. Hence, the method of this invention is suitable for use in the sub micron. Of course, it is possible to apply the present invention to the patterned process in the dual damascene, and also it is possible to the present invention to the nature changed of materials in the semiconductor devices. Also, this invention can be applied to pattern process concerning the dual damascene process used for forming the trench and the via hole at the same time by masked implantation have not been

developed at
present. Method of the present invention is the best low-K dual damascene
compatible process for deep sub-micro process.

CLPV:
performing a masked **implantation** process by way of using said photoresist layer
as a mask to form a dense region in said **dielectric** layer; and

CLPV:
performing a masked **implantation** process with energy about 20 to 100 KeV by
said photoresist layer as a mask, and **implanting into said dielectric** layer to
form a dense region with about 1000 .ANG. to 2000 .ANG. in said dielectric
layer; and

CLPV:
performing a masked **implantation** process with said first photoresist layer as a
mask to form a dense region in said first **dielectric** layer;

CLPV:
etching through said second **dielectric** layer and said first **dielectric** layer
until surface of said substrate is exposed by said dense region as an etched
barrier layer to patterning said dual damascene.

CLPV:
performing a masked **implantation** process with energy about 20 to 100 KeV by
using an ion having a dosage about 10.sup.12 to 10.sup.15 and said first
photoresist layer as a mask, and **implanting** into said first **dielectric** layer to
form an etched barrier layer with a dense region in said first **dielectric**
layer;

CLPV:
etching through said hard mask layer, said second **dielectric** layer and said

first **dielectric** layer of said predetermined etched region until a partial
surface of said substrate is exposed by said second photoresist layer as a
etched mask to form said pattern of said dual damascene in said predetermined
etched region; and

CLPV:
etching through said second **dielectric** layer and said first **dielectric** layer to
form a trench and a via hole of said dual damascene by said etched barrier
layer and said photoresist layer; and

CLPV:
etching through said second **dielectric** layer and said first **dielectric** layer to
form a trench and a via hole of said dual damascene by said dense region as an
etched barrier layer and said photoresist layer; and

CLPV:
etching through said second **dielectric** layer and said first **dielectric** layer to
form a trench and a via hole of said dual damascene by said dense region as an
etched barrier layer and said second photoresist layer; and

DOCUMENT-IDENTIFIER: US 6225204 B1
TITLE: Method for preventing poisoned vias and trenches

---------- KWIC ---------

ABPL:
A method for preventing the occurrence of poisoned trenches and vias in a dual damascene process that includes performing a densification process, such as an **implantation** process, on the surface of the exposed **dielectric** layer around the openings before the openings are filled with conductive material. The densified surface of the dielectric layer is able to efficiently prevent the occurrence of poisoned trenches and vias caused by the outgassing phenomena.

BSPR:
Referring to FIG. 1A, a substrate 100 contains a metal layer 102. A silicon nitride layer 104, which is used as an etching stop, and a silicon oxide layer 106, which is used as a **dielectric** layer, are formed on a provided substrate 100 in sequence by performing chemical vapor deposition processes. A chemical mechanical polishing process is performed to polish the dielectric layer 106 to a desired thickness, the depth of desired via plugs. Then, a silicon-oxy-nitride or silicon nitride layer 108 used as another etching stop and a silicon oxide layer 110 used as another **dielectric** layer are formed on the **dielectric** layer 106 in sequence by chemical vapor deposition processes. A chemical mechanical polishing process is performed to ensure that the thickness of the dielectric layer 110 equals the thickness of the conducting wires of the dual damascene structure to be formed in a follow-up process.

BSPR:
Referring to FIG. 1C, a portion of the etching stop 108 that is exposed within the openings 112 is removed for transferring pattern onto the etching stop 108. By using another patterned photoresist layer (not shown in figure) and the patterned etching stop 108 as masks, the **dielectric** layer 106 and 110 are etched to form via holes 116 and trenches 114. By using etching stop 108 as a mask, the etching stop 104 is patterned to expose the metal layer 102. The trenches 114 and via holes 116 compose the openings 118 of a dual damascene structure.

BSPR:
In accordance with the foregoing and other objectives of the present invention, the invention provides a method that mainly includes performing an **implantation** process on the **dielectric** layer neighboring and within the dual damascene opening before the opening is filled. The material, which includes phosphorus or arsenic, is **implanted into the dielectric** layer by a **implanter** with a angle .theta. to the normal line perpendicular to the top surface of the substrate. The entire wafer rotates horizontally during the **implantation** process to ensure that material is evenly **implanted into the dielectric** layer. The **implantation** process densifies the surface of the **dielectric** layer, so that the densified surface of the **dielectric** layer is able to efficiently prevent the occurrence of poisoned trenches and vias caused by the outgassing phenomena.

DEPR:
Referring to FIG. 2A, an etching stop 204 and a **dielectric** layer 206 are formed on a provided substrate 200, wherein the substrate 200 contains a preformed

conducting layer 202. A planarization process is performed on the dielectric layer 206, so that the thickness of the remaining dielectric layer 206 is equal to the depth of a desired via plug to be formed in a follow-up process. On the top of the planarized **dielectric** layer 206, another etching stop 208 and **dielectric** layer 210 are deposited in sequence. A planarization process is also performed on the top surface of the dielectric layer 210 after the deposition process. The thickness of the dielectric layer 210 after the planarization process is equal to the thickness of a conducting wire of the desired dual damascene structure. The dielectric layers 206 and 210 include silicon oxide, fluorine-doped silicon oxide (FSG), phosphosilicate glass (PSG), low-permittivity spin on polymer (SOP), such as aromatic-ring polymer, gel, methylsiloxane compounds, or hydrogen silsesquioxane (HSQ), or other low-permittivity materials. The etching stop 204 includes silicon nitride formed by a process such as chemical vapor deposition, and the etching stop 208 includes silicon-oxy-nitride or silicon nitride formed by a process such as chemical vapor deposition.

DEPR:
Referring next to FIG. 2B, the dielectric layer 210 is patterned to form openings 212, wherein the positions of the openings 212 correspond to the positions of the metal layer 202 underneath. The steps of forming openings 212 include depositing and patterning a photoresist layer (not shown in figure), and performing an etching process on the **dielectric** layer 210 by using the patterned photoresist layer as a mask and using the etching stop 208 as etching end point. The photoresist layer is removed after the formation of openings

212.

DEPR:
Referring to FIG. 2C, a portion of the etching stop 208 that is exposed within the openings 212 is removed for transferring pattern onto the etching stop 208. By using another patterned photoresist layer (not shown in figure) and the patterned etching stop 208 as masks, a portion of the **dielectric** layer 206 beneath the openings 212 and a portion of the **dielectric** layer 210 around the openings 212 are removed to form via holes 216 and trenches 214. Then, by using the etching stop 208 as a mask, a portion of the etching stop 204 is removed, so that the metal layer 202 is exposed by the via holes 216. The trenches 214 are further widened by the etching process as well. The trenches 214 and via holes 216 compose the openings 218 of a dual damascene structure. The etching stop 204 protects the substrate 200 and the conducting layer 202 thereon from being damaged by the etching process performed on the **dielectric** layer 206 in a case where misalignment occurs.

DEPR:
Referring next to FIG. 2D, dopants are **implanted** into the surface of the **dielectric** layers 206 and 210 neighboring and within the openings 218 by an **implanter at an implanting** angle .theta.220 away from the normal line perpendicular to the surface of the substrate. The implanting angle .theta. is about 0.degree. to 10.degree.. Preferably, the dopants, such as phosphorus boron, or arsenic, are implanted at an amount of energy of about 50 KeV to 500 KeV. In order to ensure that the dopants are evenly distributed in the exposed surface of **dielectric** 206 and 210, the wafer rotates at a constant angular speed during the **implantation** process. The densified

surface 206a and 210a are
able to prevent the occurrence of poisoned trenches and
vias during a follow-up
metallization process. In the mean time, the
low-permittivity dielectric still
provides a short RC delay.

DEPR:
It is also a specificity of the invention to prevent the
occurrence of poisoned
trenches and vias in the low-permittivity dielectrics to
improve the
reliability of a semiconductor device by performing an
implantation process to
densify a predetermined surface of the low-permittivity
dielectric.

CLPV:
performing an **implantation** process with an amount of energy
and at a angle away
from a normal line perpendicular to the substrate, for
implanting a dopant into
a portion of the **dielectric** layer exposed by the opening;
and

CLPV:
forming a first etching stop, a first **dielectric** layer, a
second etching stop,
and a second **dielectric** layer on the substrate in sequence;

CLPV:
patterning the second **dielectric** layer to form an opening
by using the second
etching stop as an etching end point, wherein the opening
is located at a
position corresponding to the conducting layer underneath;

CLPV:
removing a portion of the second etching stop exposed
within the opening for
transferring pattern onto the second etching stop;
removing a portion of the
second **dielectric** layer and a portion of the first
dielectric layer by using
the first etching stop as an etching end point and using
the second etching
stop as a mask, for transferring the opening to the first

dielectric layer to
expose the first etching stop, and widening the opening to form a trench on the
second **dielectric** layer, wherein the opening and the trench form a dual
damascene opening;

CLPV:
performing an **implantation** process at an angle with an amount of energy on the
first **dielectric** layer and second **dielectric** layer exposed within the opening;
and